f = 10 kHz, V_{CC} = 12 V, I_C (sat) = 4 mA and h_{FE} (min) = 20. Assume that $VCE_{(sat)}$ = 0.3 V and $V_{BE\ (sat)}$ = 0.7 V. **15**

(Compulsory Question)

9. Short answer type questions : **1.5×10=15**

(i) Show that a low pass circuit with a time constant acts as an Integrator.

(ii) Compare the voltage and current time base generator ? Give examples.

(iii) What is the relationship between R and the forward resistance Rf and reverse resistance Rr of the Clipping Circuit ?

(iv) List out the two regions of operation of a transistor that are used in a transistor Clipping Circuit.

(v) How many types of sampling gates are there ?

(vi) How to overcome pedestal in unidirectional sampling gates ?

(vii) Distinguish between Stable state and a Quasi Stable state in a Multivibrator.

Roll No. ..... **Total Pages : 05**

Sep-21-00061

B. Tech. EXAMINATION, 2021

Semester IV (CBCS)

PULSE SHAPING AND WAVE GENERATION

EC-404

Time : 2 Hours *Maximum Marks : 60*

The candidates shall limit their answers precisely within 20 pages only (A4 size sheets/assignment sheets), no extra sheet allowed. The candidates should write only on one side of the page and the back side of the page should remain blank. Only blue ball pen is admissible.

Note : Attempt *Four* questions in all, selecting *one* question from any of the Sections A, B, C and D. Q. No. **9** is compulsory.

Section A

1. (a) Explain differentiator circuit in detail. Show differentiatior output for step, pulse, square and ramp input. **9**

(b) Explain the response of RL circuit when a step input signal is applied. **6**

2. A limited ramp from a generator rises linearly to V_s in a time period $T_s = 0.1$ μs and remains constant for 2 μs. This signal is applied to a differentiating circuit whose time constant is 0.01 μs. The resultant pulse at the output of the differentiator has a maximum value of 15 V. What is the peak amplitude of the ramp at the output of the generator ? **15**

Section B

3. (a) Design a diode clamper circuit to clamp the positive peaks of the input signal at zero level. The frequency of the input signal is 500 Hz. **9**

(b) Justify that a clamping circuit is a dc inserter. **6**

4. (a) List the circuits of different types of shunt clippers and explain their operation with the help of their transfer characteristics. **9**

(b) What is the meaning of transmission region and attenuation region of a Clipping Circuit ? **6**

Section C

5. (a) Find the expressions for gain and minimum control voltages of a bidirectional two-diode sampling gate. **9**

(b) What is the principle of sampling gates ? Explain the operation of unidirectional diode gate. **6**

6. (a) Explain UJT in detail with construction and principle. **9**

(b) Compare two diode and four diode sampling gates. **6**

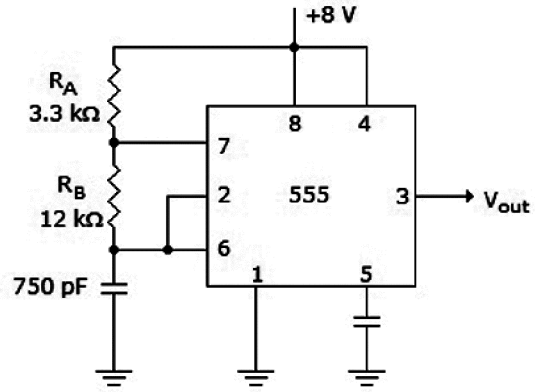
Section D

7. (a) Explain the operation of bistable multivibrator circuit with circuit diagram and waveform. Why collector catching diodes are used in multi vibrators ? **9**

(b) Explain the working of Schmitt trigger with the help of a neat circuit diagram. **6**

8. Design a collector coupled astable multivibrator to meet the following specifications :

(viii) If a diode is connected across resistor RB (positive end up) in the given figure. What is the new duty cycle of the output waveform ?



(ix) A 4-bit R/2R digital-to-analog (DAC) converter has a reference of 5 volts. What is the analog output for the input code 0101.

(x) Explain the principle operation of successive approximation ADC.